ABSTRACT OF THE DISCLOSURE

With respect to gate wires 34P arranged in a P-ROM decoder 216P, two confronting gate wires 34P to which one bit of a digital signal representing a gradation level is input with being non-inverted or inverted are paired, and the width of the gate wire that contains the upper portion of the depletion type transistor 2P (kept under ON-state at all times) and from the depletion type transistor 2P until the enhancement type transistors 1P adjacent to the depletion type transistor 2P is set to a half of the gate wire width L on the transistor 1P inside the gate wires 34P.